ABSTRACT OF THE DISCLOSURE

An apparatus for testing a memory device having a plurality of data lines includes an input circuit, a compression circuit, and an output circuit. The input circuit is adapted to receive at least a first subset of the data lines and a plurality of enable signals. Each enable signal is associated with at least one of the first subset of data lines. The compression circuit is coupled to the input circuit and is adapted to detect a predetermined pattern on the first subset of data lines. The output circuit is coupled to the compression circuit and adapted to provide at least a pass signal when the predetermined pattern is detected on the first subset of data lines. The input circuit is capable of masking at least one of the first subset of data lines from the compression circuit based on the associated enable signal. A method for testing a memory device having a plurality of data lines includes reading data present on at least a subset of the plurality of data lines. The data associated with at least one data line of the subset is masked. It is determined if the data matches a predetermined pattern. At least a pass signal is provided if the data matches the predetermined pattern.